CLAIMS

What is claimed is:

1. A method for processing an interrupt transaction in a system having a plurality of processors arranged into at least two partitions, the method comprising:

a. receiving an interrupt message;

b. decoding the interrupt message to identify an interrupt source;

c. determining whether the interrupt source is in an interrupt set;

d. dropping the interrupt if the interrupt source is not in the interrupt set;

e. determining whether the interrupt source is in a local partition and delivering the interrupt if the interrupt source is in the local partition; and

f. processing the interrupt message in accordance with at least one of a target enable register and a vector enable register if the interrupt source is in the interrupt set and not in the local partition.

2. The method according to claim 1 comprising:

decoding the interrupt message to identify an interrupt target;

determining whether the interrupt target is enabled to accept interrupts based on the target enable register; and

dropping the interrupt if the interrupt target is not enabled to accept interrupts.

3. The method according to claim 2 wherein the target enable register characterizes the enablement of the interrupt target to accept interrupts from outside the local partition and interrupts received from within the local partition are processed by the interrupt target independent of the target enable register.

4. The method according to claim 1 comprising:

decoding the interrupt message to identify an interrupt vector;

determining whether the interrupt vector is enabled based on the vector enable register; and

replacing the interrupt vector with an error vector if the interrupt vector is not enabled.

5. The method according to claim 1 comprising determining a number of interrupts having a characteristic received from the interrupt source and removing the interrupt source from the interrupt set in response to the number of interrupts.

6. The method according to claim 1 further comprising:

segregating the interrupt message into a header portion and a data portion;

decoding an interrupt source identifier from the header portion in a first processor; and

decoding an interrupt vector from the data portion in a second processor.

7. An apparatus for processing an interrupt in a system having a plurality of processors arranged into at least two partitions, the apparatus comprising:

a. an interrupt set register identifying an interrupt source from which interrupts may be accepted;

b. a partition set register identifying an interrupt source within the same partition as a interrupt target;

c. a target enable register characterizing the enablement of an interrupt target to process interrupts;

d. a vector enable register identifying interrupt vectors enabled for processing;

e. an interface module for receiving an interrupt message, the interface module comprising an interface processor for decoding the received interrupt message to identify at least one of a corresponding interrupt source, interrupt vector, and interrupt target and selectively transmitting the received interrupt message to the interrupt target responsive to at least one of the interrupt source, interrupt vector, interrupt target, interrupt set register, partition set register, target enable register, and vector enable register.

8. The method according to claim 7 wherein the interface module decodes the interrupt message to identify an interrupt target, determines whether the interrupt target is enabled to accept interrupts based on the target enable register, and drops the interrupt if the interrupt target is not enabled to accept interrupts.

9. The method according to claim 7 wherein the interface module decodes the interrupt message to identify an interrupt vector, determines whether the interrupt vector is enabled based on the vector enable register, and replaces the interrupt vector with an error vector if the interrupt vector is not enabled.

10. The apparatus according to claim 7 comprising:

an input queue for segregating the received interrupt message into a header portion and a data portion;

a first processor for receiving the header portion from the input queue and decoding an interrupt source identifier from the header portion; and

a second processor for receiving the data portion from the input queue and decoding an interrupt vector from the data portion.

11. The apparatus according to claim 10 comprising a control module with the target enable register and the vector enable register, the control module coupled to receive an interrupt source identifier and an interrupt target identifier from the first processor and an interrupt vector identifier from the second processor for controlling the first and second processors to selectively transmit the received interrupt to the interrupt target.

12. The apparatus according to claim 7 wherein the interrupt source is a processor.

13. The apparatus according to claim 7 wherein the interrupt source is a cell comprising at least one processor.

14. The apparatus according to claim 7 wherein the interrupt target is a processor.

15. The apparatus according to claim 7 wherein the interrupt target is a cell comprising at least one processor.

16. A symmetric multiprocessor system comprising a plurality of cells having at least one processor and a routing fabric for communicating a packet from one cell to another cell wherein each cell includes at least one processor and an interface to the routing fabric, the interface comprising:

a. an interrupt set register identifying a source cell from which interrupts may be accepted;

b. a partition set register identifying a cells within the same partition as a target processor;

c. a target enable register characterizing the enablement of the target processor to process interrupts;

d. a vector enable register identifying interrupt vectors enabled for processing; and

e. an interface processor for decoding a received interrupt message to identify at least one of a corresponding source cell, interrupt vector, and target processor and selectively transmitting the received interrupt message to the target processor responsive to at least one of the identified source cell, interrupt vector, target processor, interrupt set register, partition set register, target enable register, and vector enable register.

17. The system according to claim 16 wherein the interface comprises:

an input queue for segregating the received interrupt message into a header portion and a data portion;

a first processor for receiving the header portion from the input queue and decoding a source cell identifier from the header portion; and

a second processor for receiving the data portion from the input queue and decoding an interrupt vector from the data portion.

18. A computer readable media comprising computer readable code for instructing a computer to process an interrupt in a system having a plurality of processors arranged into at least two partitions, an interface module in one of the partitions for receiving an interrupt message, an interrupt set register identifying an interrupt source from which interrupts may be accepted, a partition set register identifying an interrupt source within the same partition as the interface module, a target enable register identifying an interrupt target enabled to process interrupts, and a vector enable register identifying interrupt types enabled to be processed comprising:

a. receiving an interrupt message identifying an interrupt source, an interrupt target, and an interrupt vector;

b. dropping the interrupt if the interrupt source is not identified in the interrupt set as an element from which interrupts may be accepted;

c. dropping the interrupt if the interrupt source is identified in the interrupt set as an element from which interrupts may be accepted, the interrupt source is not in the same partition as the interface module, and the interrupt target is not identified as an element enabled to process interrupts; and

d. transmitting the interrupt to the interrupt target if interrupt source is not dropped in one of steps (b) and (c).

19. A system for processing an interrupt in a system having a plurality of processors in at least two partitions comprising:

a. first means for receiving an interrupt message identifying an interrupt source, an interrupt target, and an interrupt vector;

b. second means for storing an interrupt set identifying an element from which interrupts may be accepted;

c. third means for storing a partition set identifying an element within the same partition as the interrupt target;

d. fourth means for storing a target enable register identifying an element enabled to process interrupts;

e. fifth means for storing a vector enable register identifying interrupt vectors enabled to be processed; and

f. sixth means for selectively transmitting the received interrupt to the interrupt target responsive to at least one of the interrupt source, interrupt type, interrupt target, interrupt set, partition set, target enable register and vector enable register.